REMARKS

Claims 1-10 are currently pending in the subject application. By this amendment, the specification is amended to correct a typographical error. No new matter is added by the amendment to the specification.

Applicants appreciate the Examiner's acknowledgement of Applicants' claim for foreign priority and receipt of a certified copy of the priority document.

Applicants further appreciate the Examiner's indication of allowable subject matter in claims 4 and 5.

Claims 1-10 are presented to the Examiner for further prosecution on the merits.

Reconsideration of this application is respectfully requested in view of the foregoing amendment and following remarks.

In the outstanding Office Action, the drawings are objected to. The specification has been amended to overcome this objection. Accordingly, withdrawal of the objection is requested.

In the outstanding Office Action, claim 1 is rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No.: 6,509,851 to Clark et al., (hereinafter, "Clark"), claims 2, 3 and 6-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Clark, and claims 8-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in view of Clark.

These rejections are respectfully traversed for at least the reasons set forth below.

U.S. Patent No.: 6,509,851 to Clark, et al. is cited as the primary reference in the outstanding rejections. However, U.S. Patent No.: 6,509,851 to Clark, et al. has a U.S. filing date of March 30, 2000.

The subject application claims priority under 35 U.S.C. § 119(b) of Japanese Patent Application No. 2000-030803, filed on February 8, 2000. The claim for priority and receipt of all certified copies of the priority documents have been acknowledged by the Office. Therefore, to perfect priority under 35 U.S.C. §119(b), an English language translation of the certified copy of the priority document and an executed statement by the translator that the translation is accurate are included herewith.

Accordingly, since the subject application has an effective U.S. filing date that precedes the filing date of Clark, it is respectfully requested that the rejections based on the Clark reference be withdrawn.

CONCLUSION

For at least the above reasons, it is respectfully submitted that claims 1-10 are in condition for allowance and a notice to such effect is respectfully requested. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The fee for this extension may

be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referencing Client Matter No. 100353-00040.

Respectfully submitted,

ARENT FOX, PLLC

Michele L. Connell
Registration No. 52,763

Customer No. 004372
ARENT FOX PLLC
1050 Connecticut Avenue, N.W.,
Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810

I, Tadahiko Itoh, a Patent Attorney of Tokyo, Japan having my office at 32nd Floor, Yebisu Garden Place Tower, 20-3 Ebisu 4-Chome, Shibuya-Ku, Tokyo 150-6032, Japan do solemnly and sincerely declare that I am the translator of the attached English language translation and certify that the attached English language translation is a correct, true and faithful translation of Japanese Patent Application No. 2000-030803 to the best of my knowledge and belief.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Tadahiko ITOH
Patent Attorney
ITOH International Patent Office
32nd Floor,
Yebisu Garden Place Tower,
20-3 Ebisu 4-Chome, Shibuya-Ku,
Tokyo 150-6032, Japan

PATENT OFFICE

JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this office.

Date of Application: February 8, 2000

Application Number: Japanese Patent Application No. 2000-030803

Applicant(s) FUJITSU LIMITED

January 5, 2001

Commissioner,
Patent Office Kouzo Oikawa (Seal)

Certificate No.2000-3109956

(Document Name)	Application for Patent
(Reference Number)	9903237
(Date of Submission)	February 8, 2000
(Destination)	Commissioner of Patent Office Mr. Takahiko Kondo
(IPC)	H01L 27/00 H04L 13/10
(Title of the Invention)	DATA INPUT CIRCUIT AND SEMICONDUCTOR DEVICE UTILIZING THE DATA INPUT CIRCUIT
(Number of Claims)	9
(Inventor)	
(Residence or Address)	c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, Japan
(Name)	Kazuyuki Kanazashi
(Applicant for Patent)	
(Identification Number)	000005223
(Name)	FUJITSU LIMITED
(Attorney)	
(Identification Number)	100070150
(Residence or Address)	32nd Floor, Yebisu Garden Place Tower 20-3, Ebisu 4-chome, Shibuya-ku Tokyo, Japan
(Patent Attorney)	
(Name)	Tadahiko Itoh
(Telephone Number)	03-5424-2511
(Identification of Official Fees)	
(Prepayment Ledger Number)	002989
(Amount Paid)	¥ 21,000
(Lists of Submitted Documents)	
(Document Name)	Specification 1
(Document Name)	Drawing 1
(Document Name)	Abstract 1
(Number of General Power of Attorney)	9704678
(Proof Requested or Not)	Requested

[Name of Document] SPECIFICATION

[Title of Invention] DATA INPUT CIRCUIT AND SEMICONDUCTOR DEVICE UTILIZING THE DATA INPUT CIRCUIT

[Claims]

1. A data input circuit converting input serial data to n-bit parallel data, and outputting the n-bit parallel data by following an address signal, said data input circuit comprising:

data shifting means including a plurality of columns, and sequentially shifting the input serial data through the plurality of columns; and

selection means selecting a column among the plurality of columns as an input column by following the address signal, wherein the input serial data is inputted to said data shifting means through the input column.

2. The data input circuit as claimed in claim 1, wherein said data shifting means includes 2n-l columns, and said selection means selects the input column through which the input serial data is inputted to said data shifting means.

3. The data input circuit as claimed in claim 2, wherein said data shifting means executes a logical arithmetic operation on a combination of outputs of n columns storing the input serial data and outputs of n-l columns not storing the input serial data, thereby converting the input serial data to the n-bit parallel data following the address signal.

4. The data input circuit as claimed in claim 1 wherein:

said data shifting means includes n columns, and a feed-back function feeding the input serial data stored in a n^{th} column of said data shifting means back to a first column of said data shifting means; and

said selection means selects the input column by following the address signal so as to input the input serial data to said data shifting means.

5. The data input circuit as claimed in claim 4, wherein said data shifting means converts the input serial data to the n-bit parallel data following the address signal by outputting the input serial data from the n columns storing the input serial data.

6. The data input circuit as claimed in claim 3 or 5 wherein, said input serial data is inputted by n bits to said data shifting means, and a destination of each bit is determined by the address signal.

7. The data input circuit as claimed in claim 1, wherein:

said data shifting means includes a plurality of data storage means as the plurality of columns, and a plurality of switching means controlled by said selection means, said plurality of data storage means storing the input serial data; and

said selection means selects a data storage means as the input column among the plurality of data storage means by controlling the plurality of switching means.

8. A semiconductor device including a data input circuit converting input serial data to n-bit parallel data, and outputting the n-bit parallel data by following an address signal, said semiconductor device comprising:

data shifting means including a plurality of columns, and sequentially shifting the input serial data through the plurality of columns; and

selection means selecting a column among the plurality of columns as an input column by following the address signal, wherein the input serial data is inputted to said data shifting means through the input column.

9. The semiconductor device as claimed in claim 8, wherein:

said data shifting means includes a plurality of data storage means as the plurality of columns, and a plurality of switching means controlled by said selection means, said plurality of data storage means storing the input serial data; and

said selection means selects a data storage means as the input column among the plurality of data storage means by controlling the plurality of switching means.

[Detailed Description of the Invention]

[Technical Field of the Invention]

The present invention relates to a data input circuit and a semiconductor device utilizing the data input circuit. The present invention more particularly relates to a data input circuit receiving serial data synchronously to a clock, and converting the serial data to parallel data, and a semiconductor device utilizing the data input circuit.

[The Conventional Art]

Some semiconductor devices include an input circuit converting serial data supplied from outside the semiconductor devices to parallel data, and outputting the parallel data to a data bus by following an address signal. The input circuit creates a plurality of address signals from a single address signal supplied in accordance with a command signal, and outputs the parallel data to the data bus by following the plurality of address signals.

FIG. 1 is a diagram showing a configuration of a conventional input circuit. An input circuit 100 includes an input buffer 110, a shift register 120 (a data-acquiring buffer) and a data switch unit 130. The data switch unit 130 includes switches 131 through 134. Additionally, FIGS. 2A and 2B are diagrams showing signal processes performed by the input circuit 100. It should be noted that FIGS. 1, 2A and 2B show a case in which data is

supplied to the input circuit 100 by a DDR (Double Data Rate) method supplying the data with a frequency twice as higher than that of an external clock, for instance.

An address signal A2 is initially supplied to the input circuit 100 with a data-write command as shown in FIG. 2A. The address signal A2 is one of address signals AO, Al, A2 and A3 expressed by a combination of the least two significant bits (Yl, Y0) of an address.

Additionally, the address signal A2 supplied with the data-write command to the input circuit 100 indicates that input data is supplied to the input circuit 100 in order of data A2, data A3, data A0 and data Al continuously after the address signal A2 and the data-write command have been supplied.

To be concrete, the data A2, A3, A0 and Al is supplied through the input buffer 110 to the shift register 120 in the order of the data A2, A3, A0 and Al by following a frequency of an internal clock CLK1. The shift register 120 shifts data supplied thereto one by one as shown in FIG. 2B.

For example, if an address signal supplied with the data-write command to the input circuit 100 is the address signal A2, the shift register 120 stores the data A2, A3, A0 and Al respectively in areas No, Nl, N2 and N3 of the shift register 120.

The areas No, Nl, N2 and N3 of the shift register 120 are respectively connected to the switches 131, 132, 133 and 134 included in the data switch unit 130. The switches 131 through 134 are connected to data buses AO through A3. The input circuit 100 outputs input data to a data bus corresponding to a supplied address signal by controlling the switches 131 through 134 by following the supplied address signal.

For example, in the case in which an address signal supplied with the data-write command to the input circuit 100 is the address signal A2, the areas NO, Nl, N2 and N3 are respectively connected with the data buses A2, A3, AO and Al as shown in FIG. 2C.

As described above, the input circuit 100 creates a group of four address signals (e.g., A0~A3), each address signal corresponding to a combination of the least two significant bits of an address, automatically recognizes an order of four input data (e.g., A2, A3, A0, A1), and outputs the four input data to their corresponding data buses. Such an operation is called a 4N operation.

FIG. 3 is a diagram showing a configuration of another conventional input circuit. An input circuit 200 shown in FIG. 3 includes the input buffer 110, data-acquiring buffers 140 (N0) through 143 (N3), and an address counter 150. Additionally, FIGS. 4A, 4B and 4C are diagrams showing signal processes performed by the input circuit 200. The input circuit 200 achieves the 4N operation by controlling a data-acquiring clock supplied to the

data-acquiring buffers 140 through 143 that are provided for the input data A0 through A3.

The address signal A2 is initially supplied to the input circuit 200 with the data-write command as shown in FIG. 4A. The address counter 150 generates data-acquiring clocks 1 through 4 by following the address signal A2 as shown in FIG. 4B, and supplies the data-acquiring clocks to the data-acquiring buffers 140 through 143.

To be concrete, the data-acquiring clocks 1, 2, 3 and 4 are respectively supplied to the data-acquiring buffers 140, 141, 142 and 143. The data-acquiring buffers 140 through 143 obtain the input data A0 through A3 respectively at rising edges of the data-acquiring clocks 1 through 4 as shown in FIG. 4C. Subsequently, the data-acquiring buffers 140 through 143 outputs obtained input data, for example, the input data A0 through A3 respectively to the data buses A0 through A3.

[Problem to be Solved by the Invention]

However, the input circuit 100 of FIG1 needs to have a data switch unit 130 having numerous switches.

For example, in the case of automatically recognizing the order of 2^n sets of input data as a combination of 2^n address signals corresponding to a combination of lower n bits, and outputting data to a corresponding data bus, the data switch unit 130 needs to be provided with $(2^n)^2$ switches (e.g., in the case of the 4N operation, 4^2 switches are required).

Thereby, the circuit area is increased and the circuit configuration becomes complicated.

Also, the input circuit 200 shown in FIG. 3 needs to generate the data-acquiring clocks at the highest frequency possible. However, since a logical circuit such as the address counter 150 must generate the data-acquiring clocks, speed up of processes executed by the input circuit 200 is hard.

Accordingly, it is a general object of the present invention to provide a data input circuit and a semiconductor device utilizing the data input circuit. A more particular object of the present invention is to provide a data input device speeding up its processing speed with a simplified circuit structure reducing a circuit size, and a semiconductor device utilizing the data input device, in which the disadvantages. described above are eliminated.

[Means Used to Solve the Problem]

The above-described object of the present invention is achieved by a data input circuit as claimed in claim 1 converting input serial data to n-bit parallel data, and outputting the n-bit parallel data by following an address signal, the data input circuit including data shifting means (e.g., shift register 14 of FIG5) including a plurality of

columns, and sequentially shifting the input serial data through the plurality of columns; and selection means (e.g., input point selector 12 of FIG5) selecting a column among the plurality of columns as an input column by following the address signal, wherein the input serial data is inputted to the data shifting means through the input column.

The selection means selects the column to input the input serial data to the data shifting unit. Subsequently, the data shifting means obtains the input serial data, and shifts the input serial data so that the input serial data stored in each column of the data shifting unit can be converted into parallel data and outputted to its corresponding destination.

A data input circuit of claim 2 is characterized in that the data shifting means includes 2n-l columns, and the selection means selects the input column through which the input serial data is inputted to said data shifting means.

By arranging the data shifting means to include 2n-1 columns and selecting a column through which input data are input, input serial data stored in each column of the data shifting means can be converted into parallel data and outputted to its corresponding destination.

A data input circuit of claim 3 is characterized in that the data shifting means executes a logical arithmetic operation on a combination of outputs of n columns storing the input serial data and outputs of n-l columns not storing the input serial data, thereby converting the input serial data to the n-bit parallel data following the address signal.

When the data shifting means includes 2n-1 columns, columns not storing input serial data are created, and thereby, necessary outputs may be generated by performing a predetermined logical arithmetic operation with respect to the columns storing the serial data and columns not storing the serial data.

A data input circuit of claim 4 is characterized in that the data shifting means (e.g., shift register 40 of FIG8) includes n columns, and a feed-back function feeding the input serial data stored in a n^{th} column of said data shifting means back to a first column of said data shifting means; and the selection means selects the input column by following the address signal so as to input the input serial data to said data shifting means.

By including a feed-back, the data shifting means may be made up of n columns even in the case where the selection means selects the column to input the input serial data to the data shifting unit.

A data input circuit as claimed in claim 5 is characterized in that the data shifting means converts the input serial data to the n-bit parallel data following the address signal by outputting the input serial data from the n columns storing the input serial data.

By selecting the column to input the input serial according to the address signal,

the outputs of n columns may be converted into parallel data according to their addresses.

A data input circuit as claimed in claim 6 is characterized in that the input serial data is inputted by n bits to said data shifting means, and a destination of each bit is determined by the address signal.

By selecting the column to input the input serial according to the address signal, the outputs of n columns may be converted into parallel data according to their addresses when serial data comprising n bits as one unit are input to the data shifting means.

A data input circuit as claimed in claim 7 is characterized in that the data shifting means includes a plurality of data storage means as the plurality of columns, and a plurality of switching means controlled by said selection means, said plurality of data storage means storing the input serial data; and the selection means selects a data storage means as the input column among the plurality of data storage means by controlling the plurality of switching means.

By providing the data shifting means with the switching means and the data storage means, the column to which serial data are to be input may be selected from plural data storage means.

A semiconductor device as claimed in claim 8 including a data input circuit converting input serial data to n-bit parallel data, and outputting the n-bit parallel data by following an address signal, is characterized by comprising:

data shifting means including a plurality of columns, and sequentially shifting the input serial data through the plurality of columns; and

selection means selecting a column among the plurality of columns as an input column by following the address signal, wherein the input serial data is inputted to said data shifting means through the input column.

By implementing the data input circuit of the present invention in a semiconductor device, miniaturization of the circuit and increased speed in the serial/parallel data conversion may be realized.

Also, a semiconductor device as claimed in claim 9 is characterized in that the data shifting means includes a plurality of data storage means as the plurality of columns, and a plurality of switching means controlled by said selection means, said plurality of data storage means storing the input serial data; and the selection means selects a data storage means as the input column among the plurality of data storage means by controlling the plurality of switching means.

By providing the data shifting means with the switching means and the data storage means, the column to which serial data are to be input may be selected from plural

data storage means.

It is noted that the references in parentheses in the above description are merely examples provided to facilitate understanding of the present invention.

[Embodiments of the Invention]

A description will now be given of preferred embodiments of the present invention, with reference to the accompanying drawings.

FIG 5 is a diagram showing a configuration of an input circuit 1 according to a first embodiment of the present invention. The input circuit 1 shown in FIG 5 includes an input buffer 10, an input-point selector (a decoder) 12, a shift register (a data-acquiring buffer) 14, inverters 16 through 20, and NAND gates 21 through 23. The input circuit 1 generates a plurality of address signals from a single address signal supplied in accordance with a command signal, converts serial data supplied from outside the input circuit 1 to parallel data, and outputs the parallel data to a data bus by following the plurality of address signals.

A description will now be given of a case in which the input circuit 1 creates a group of four address signals, for example, address signals A0 through A3, each address signal corresponding to a combination of the least two significant bits of an address, automatically recognizes an order of four input data, and outputs the four input data to their corresponding data buses AO through A3.

The shift register 14 includes seven columns that are N3, N2, Nl, N0, N3', N2' and Nl', and shifts input data from the column N3 toward the column Nl'. If the input circuit 1 uses a group of 2n address signals in which a number wn" is a natural number, the shift register 14 includes 2n+l-1 columns.

The input-point selector 12 controls a data input point of the shift register 14 by following an address signal inputted thereto. For example, the input-point selector 12 selects the column Nl as the data input point of the shift register 14 in a case in which the address signal A2 is supplied to the input circuit 1 with a data-write command.

The columns N3 and N3' of the shift register 14 are connected to the NAND gate 21 whose output terminal is connected to the data bus A3 through the inverter 16. Similarly, the columns N2 and N2' of the shift register 14 are connected to the NAND gate 22 whose output terminal is connected to the data bus A2 through the inverter 17. The columns Nl and Nl' of the shift register 14 are connected to the NAND gate 23 whose output terminal is connected to the data bus Al through the inverter 18. Additionally, the column N0 of the shift register 14 is connected to the data bus A0 through the inverters 20 and 19.

FIGS. 6A and 6B are diagrams showing signal processes performed by the input circuit 1, according to the first embodiment.

The address signal A2 is initially supplied with the data-write command to the input circuit 1 as shown in FIG 6A. The address signal A2 is one of the address signals A0 through A3 expressed by a combination of the least two significant bits (Y1, YO) of an address.

The address signal A2 supplied with the data-write command indicates that the input data is supplied to the input circuit 1 in order of the input data A2, A3, A0 and A1 after the address signal A2 is supplied thereto. If the address signal A4 is supplied with the data-write command to the input circui t 1, the input data is suppli'ed to the input circuit 1 in order of the input data A4, A0, A1 and A2 after the address signal A4 is supplied thereto.

The input-point selector 12 selects the column N1 as a data input point of the shift register 14 by following the supplied address signal A2 as shown in FIG 6B. Subsequently, the input data is supplied to the shift register 14 through the input buffer 10 by following a frequency of an internal clock CLK1 in the order of the input data A2, A3, A0 and A1.

Since the input-point selector 12 selects the column N1 of the shift register 14 as the data input point, the input data supplied from the input buffer 10 is inputted to the column N1 continuously in the order of the input data A2, A3, AO and A1. As a result, the columns N1, NO, N3' and N2' store respectively the input data A1, A0, A3 and A2 as shown in FIG 6B. The columns N1', N2 and N3 not storing the input data store a predetermined value, for example, a high-level signal or value as shown in FIG 5.

The input data Aq stored in the column NO of the shift register 14 is outputted to the data bus AO through the inverters 20 and 19. The input data A1 stored in the column N1 of the shift register 14 and a value stored in the column N1' of the shifter register 14 are supplied to the NAND gate 23, whose output is outputted to the data bus A1 through the inverter 18.

Similarly, the input data A2 stored in the column N2' of the shift register 14 and a value stored in the column N2 of the shifter register 14 are supplied to the NAND gate 22, whose output is outputted to the data bus A2 through the inverter 17. The input data A3 stored in the column N3' of the shift register 14 and a value stored in the column N3 of the shifter register 14 are supplied to the NAND gate 21, whose output is outputted to the data bus A3 through the inverter 16.

For instance, the values stored in the columns N1', N2 and N3 are high-level signals, the input data A1 stored in the column N1, the input data A2 stored in the column N2' and the input data A3 stored in the column N3' are outputted to the data bus A1, A2

and A3 respectively.

FIG 7 is a diagram showing a configuration of the shift register 14, according to the first embodiment. The shift register 14 shown in FIG 7 includes switches SWO through SW3, flip-flops FFO through FF3 and FF1' through FF3', inverters 30 trough 33, and NOR gates 34 through 37.

The input-point selector 12 outputs a signal selecting the column N1 of the shift register 14 to the shift register 14 by following the address signal A2 after receiving the address signal A2 and the data-write command as shown in FIG 6A.

Specifically, the input-point selector 12 outputs a high-level signal from its output terminal N(A2) to the switch SW2 of the shift register 14, and low-level signals from the other terminals N(AO), N(A1) and N(A3) respectively to the switches SWO, SW1 and SW3. The switch SW2 connects to a side "b" after receiving the high-level signal from the output terminal N(A2) of the input-point selector 12. Each of the switches SW1 and SW3 connects to a side "a" after receiving the low-level signal respectively from the output terminals N(AO) and N(A3) of the input-point selector 12. Additionally, the switch SWO becomes disconnected after receiving the low-level signal from the output terminal N(AO) of the input-point selector 12.

Consequently, the input data A2, A3, A0 and A1 is inputted continuously to the flip-flop FF1 of the shift register 14 through the switch SW2 connected to the side "b", and is shifted one after another toward the flip-flop FF1'. Because of shifting the input data, the shift register 14 stores the input data A1, A0, A3 and A2 respectively in the flip-flops FF1, FFO, FF3' and FF2'. Additionally, the shift register 14 is configured so as to supply a SET signal to the flip-flops FF3, FF2 and FF1', which do not store the input data.

According to the first embodiment, the input circuit 1 can select a data input point (a column) of the shift register 14 by following an address signal by use of the input-point selector 12, thereby enabling conversion of supplied serial data to parallel data and output of the parallel data to its corresponding data bus or the like.

FIG 8 is a diagram showing a configuration of an input circuit 2 according to a second embodiment of the present invention. The input circuit 2 shown in FIG 8 includes the input buffer 10, the input-point selector 12, a shift register 40, and inverters 42 through 49.

The shift register 40 includes four columns N3, N2, N1 and NO, and shifts input data in a direction from the column N3 to the column N0. Additionally, the shift register 40 is provided with a feedback loop so that input data shifted to the column NO is fed back to the column N3 at the next shift. The shift register 40 needs to have 2^n columns in which a number "n" is a natural number if a group of 2^n address signals is provided thereto.

The input-point selector 12 controls a data input point of the shift register 40 by following an address signal inputted thereto similarly to the shift register 14 described in the first embodiment.

The columns N3, N2, N1, N0 of the shift register 40 are connected to the data bus A3, A2, A1, A0, respectively, through the inverters.

FIGS. 9A and 9B are diagrams showing signal processes performed by the input circuit 2, according to the second embodiment.

The address signal A2 and the data-write command are supplied to the input circuit 2 as shown in FIG 9A. The input-point selector 12 selects the column N1 as a data input point of the shift register 40 as shown in FIG 9A. Subsequently, the input data is supplied to the shift register 40 through the input buffer 10 by following the frequency of the internal clock CLK1 in order of the input data A2, A3, A0 and A1.

Since the input-point selector 12 selects the column N1 of the shift register 40 as the data input point of the shift register 40, the input data A2, A3, A0 and A1 is continuously inputted to the shift register 40 from the column N1. The input data A2 initially enters the column N1, and is stored in the column N1.

At the next step, the input data A3 enters the column Nl, and is stored in the column N1. Meanwhile, the input data A2 is shifted to the column No, and is stored in the column N0. Subsequently, at the time the input data A0 is entering the column N1, the input data A3 is shifted to the column NO as well as the input data A2 is fed back to the column N3. Thus, after the input data A2, A3, AO and A1 is inputted from the column N1 to the shift register 40 one by one, the shift register 40 stores the input data A3, A2, A1 and A0 respectively in the .columns N3, N2, N1 and No.

Subsequently, the input data A3, A2, A1 and A0 stored respectively in the columns N3, N2, N1 and N0 of the shift register 40 are outputted respectively to the data buses A3, A2, A1 and A0 through two inverters.

FIG 10 is a diagram showing a configuration of the shift register 40, according to the second embodiment. The shift register 40 shown in FIG 10 includes switches SWO through SW3, and flip-flops FFO through FF3.

After receiving the address signal A2 with the data-write command as shown in FIG 9A, the input-point selector 12 outputs a control signal to set the data input point of the shift register 40 to the column N1 by following the address signal A2.

To be concrete, the input-point selector 12 outputs a high-level signal (HIGH) from its output terminal N(A2), and low-level signals (LOW) from its output terminals N(AO), N(A1) and N(A3), as shown in FIG 9A. Since the switch SW2 is connected to

the output terminal N(A2) of the input-point selector 12, and receives the high-level signal therefrom, the switch SW2 is connected to a side "b".

Additionally, the switches SW0, SW1 and SW3 are respectively connected to the output terminals N(AO), N(A1) and N(A3) of the input-point selector 12, and receive the low-level signal, the switches SWO, SW1 and SW3 are connected to their sides "a".

Accordingly, the input data supplied from the input buffer 10 is inputted to the flip-flop FF1 through the switch SW2 connected to the side "b". Subsequently, the input data A2, A3, A0 and A1 inputted to the shift register 40 from the flip-flop FF1 is shifted in order through the switches SW1, SW0 and SW3, which are connected to the sides "a". Input data stored in the flip-flop FFO is shifted when new input data is inputted to .the flip-flop FF1.

As described above, the shift register 40 can select a data input point by following an address signal supplied with the data-write command, and can output supplied input data to their corresponding data buses. Additionally, the input circuit 2 according to the second embodiment stores input data in all the flip-flops provided in the shift register 40, and thus does not have to provide a SET signal necessary in the fist embodiment to the shift register 40, thereby achieving objects of the present invention with a simpler circuit structure.

Additionally, the input circuit 2 includes a feed-back loop in the shift register 40, and thus does not need to include no more than n columns in the shift register 40 for generating n-bit parallel data. According to the first and second embodiments, the shift registers 14 and 40 include a plurality of switches and flip-flops, thereby enabling input of serial data to the shift registers 14 and 40 through the plurality of flip-flops.

FIG. 11 is a block diagram showing a configuration of a semiconductor device 3 utilizing the input circuit 1 or 2 according to the present invention. The semiconductor device 3 shown in FIG. 11 is a SDRAM (Synchronous Dynamic Random Access Memory) utilizing a delayed-write method and the input circuit 1 or 2 according to the present invention. Data inputted to the semiconductor device 3 is supplied to a serial-parallel converter 52 through a buffer/register 50, the serial-parallel converter 52 corresponding to the input circuit 1 or 2.

The serial-parallel converter 52 can generate a plurality of address signals from a single address signal supplied in accordance with a command signal, can convert serial data to parallel data, and can output the parallel data to a common data bus. It should be noted that the single address signal necessary for processes performed by the present invention is supplied to the serial-parallel converter 52.

Thus, by applying the input circuit 1 or 2 to the semiconductor device 3, the semiconductor device 3 can reduce its circuit size, and can convert supplied serial data to parallel data speedily as well as can output the parallel data to a data bus.

[Advantages of the Invention]

As describe above, the present invention provides a method of converting serial data to parallel data by inputting the serial data to a data shifting method from a column of the data shifting method determined by use of an address signal, and outputting the parallel data to its corresponding data bus.

Therefore, the present invention can provide a data input device speeding up its processing speed with a simplified circuit structure whose circuit size is reduced, and a semiconductor device utilizing the data input device. The above description is provided in order to enable any person skilled in the art to make and use the invention and sets forth the best mode contemplated by the inventors of carrying out the invention.

[Brief Description of the Drawings]

FIG 1: diagram showing a configuration of a conventional input circuit

FIG 2: diagrams showing signal processes performed by the conventional input circuit

FIG 3: diagram showing a configuration of another conventional input circuit

FIG 4: diagrams showing signal processes performed by the conventional input circuit shown in FIG 3

FIG 5: diagram showing a configuration of an input circuit according to a first embodiment of the present invention

FIG 6: diagrams showing signal processes performed by the input circuit according to the first embodiment

FIG 7: diagram showing a configuration of a shift register, according to the first embodiment

FIG 8:diagram showing a configuration of the input circuit according to a second embodiment of the present invention

FIG 9: diagrams showing signal processes performed by the input circuit according to the second embodiment

FIG 10: diagram showing a configuration of the shift register, according to the second embodiment

FIG 11: block diagram showing a configuration of a semiconductor device utilizing the input circuit according to the present invention

[Description of Reference Symbols]

1 input circuit

10 input buffer

12 input point selector

14, 40 shift register

16~20, 30~33, 42~49 inverter circuit

21~23 NAND circuit

34~37 NOR circuit

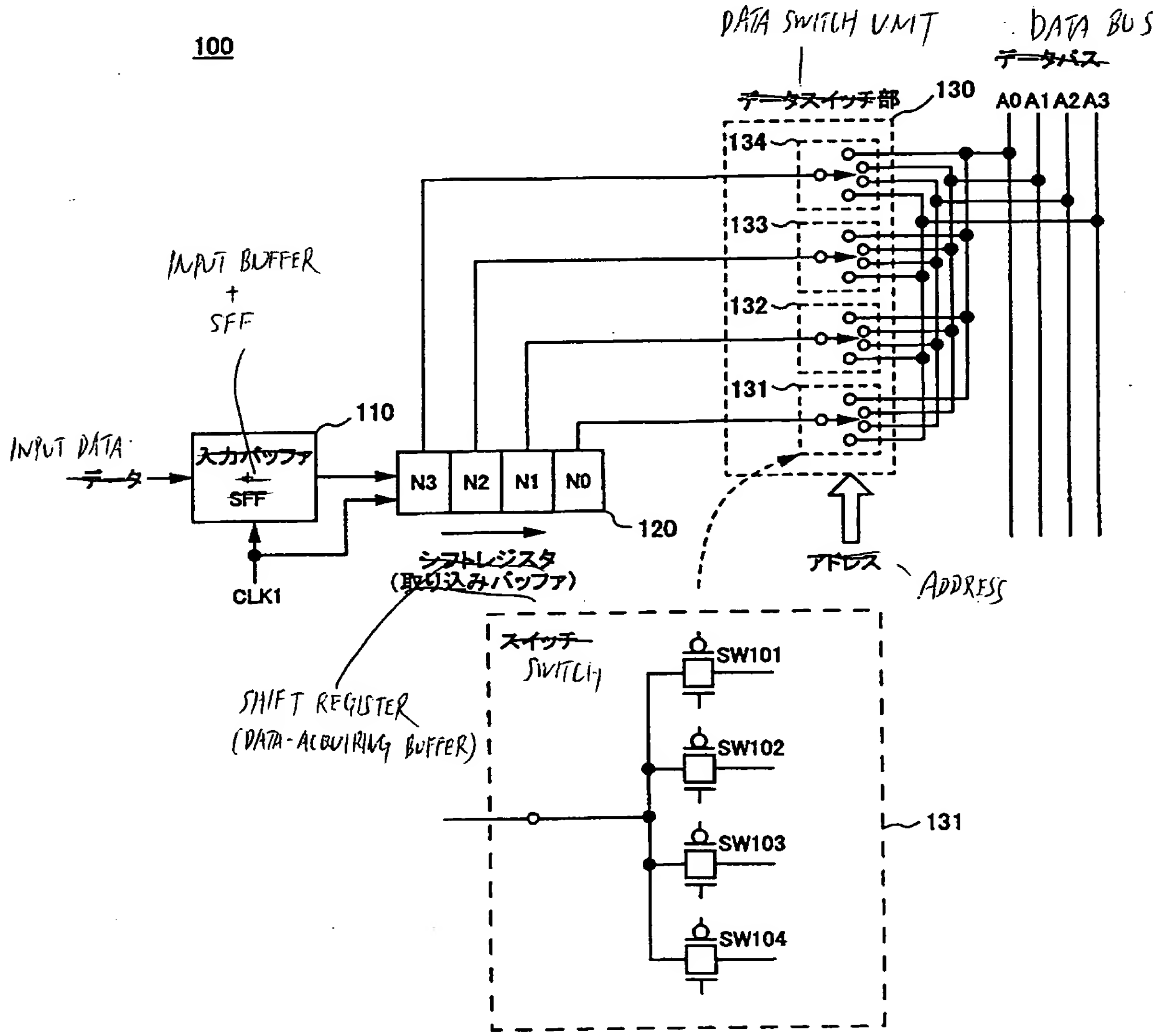
50 buffer/register

52 serial/parallel converter

~~【書類名】~~ 図面 [Document name] Drawing

~~【図１】~~ FIG. 1

~~入力回路の一例の構成図~~



~~【図２】~~

~~入力回路の動作を説明する図~~

FIG. 2A

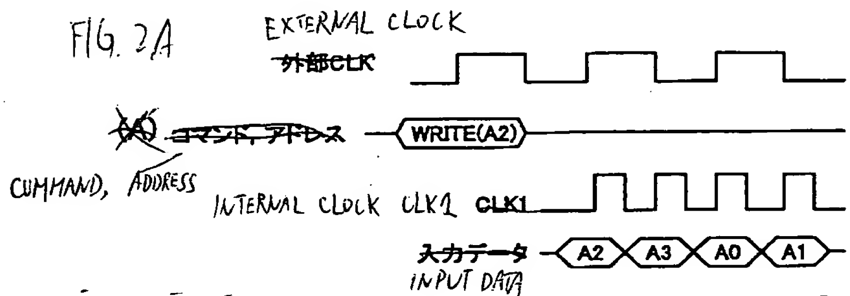
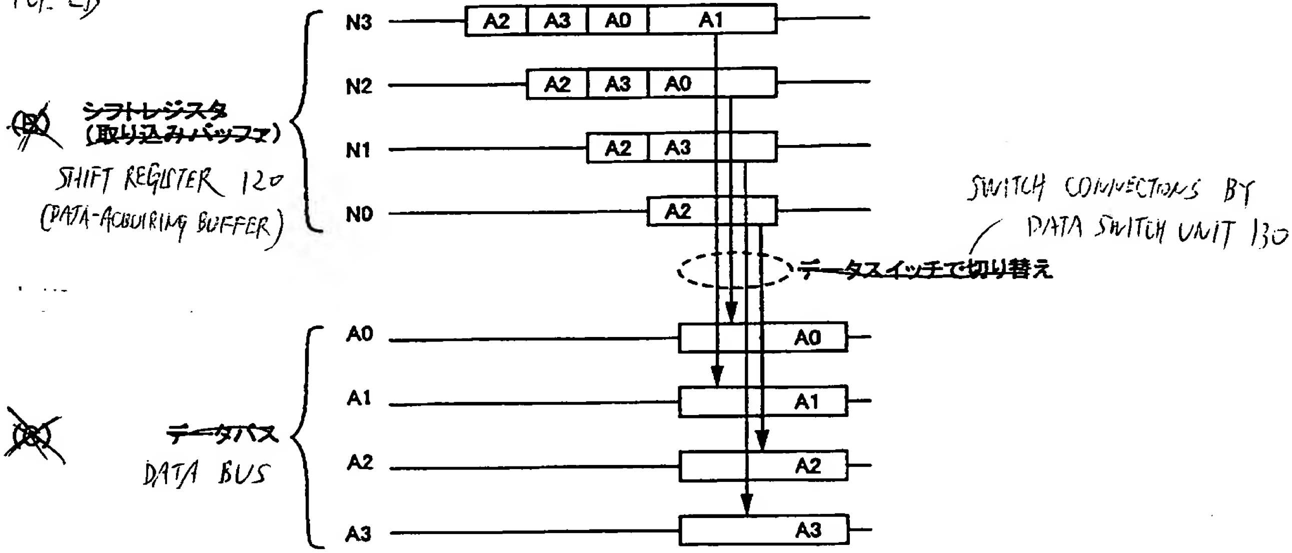


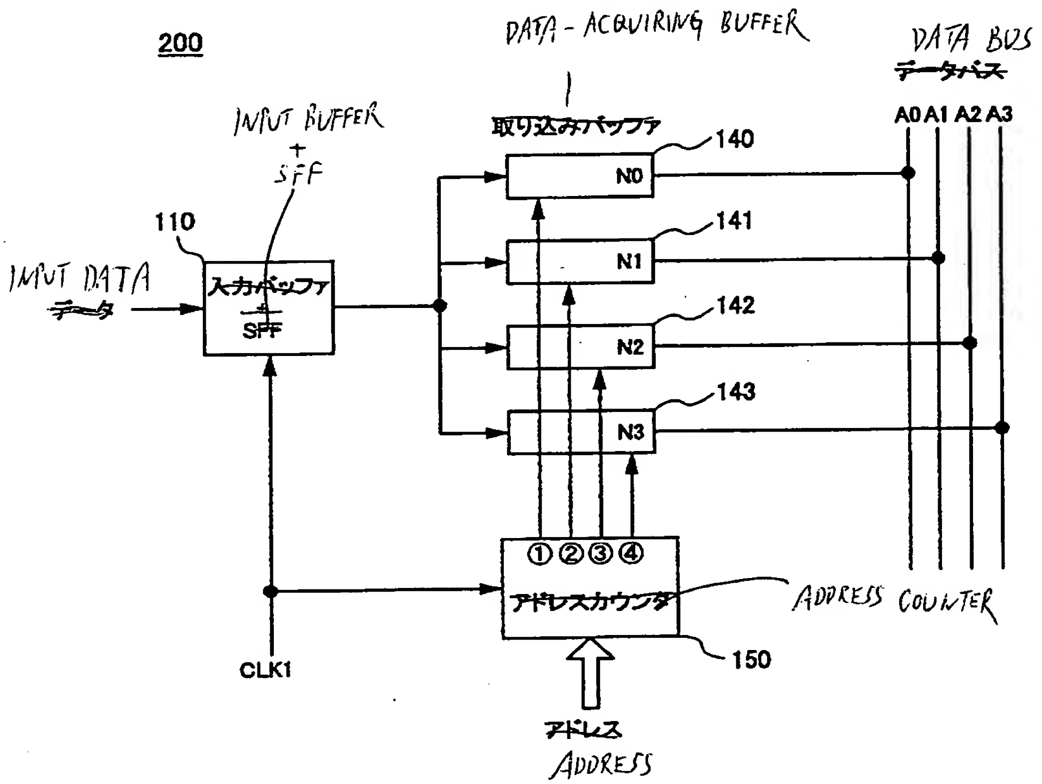
FIG. 2B



【~~図３~~】

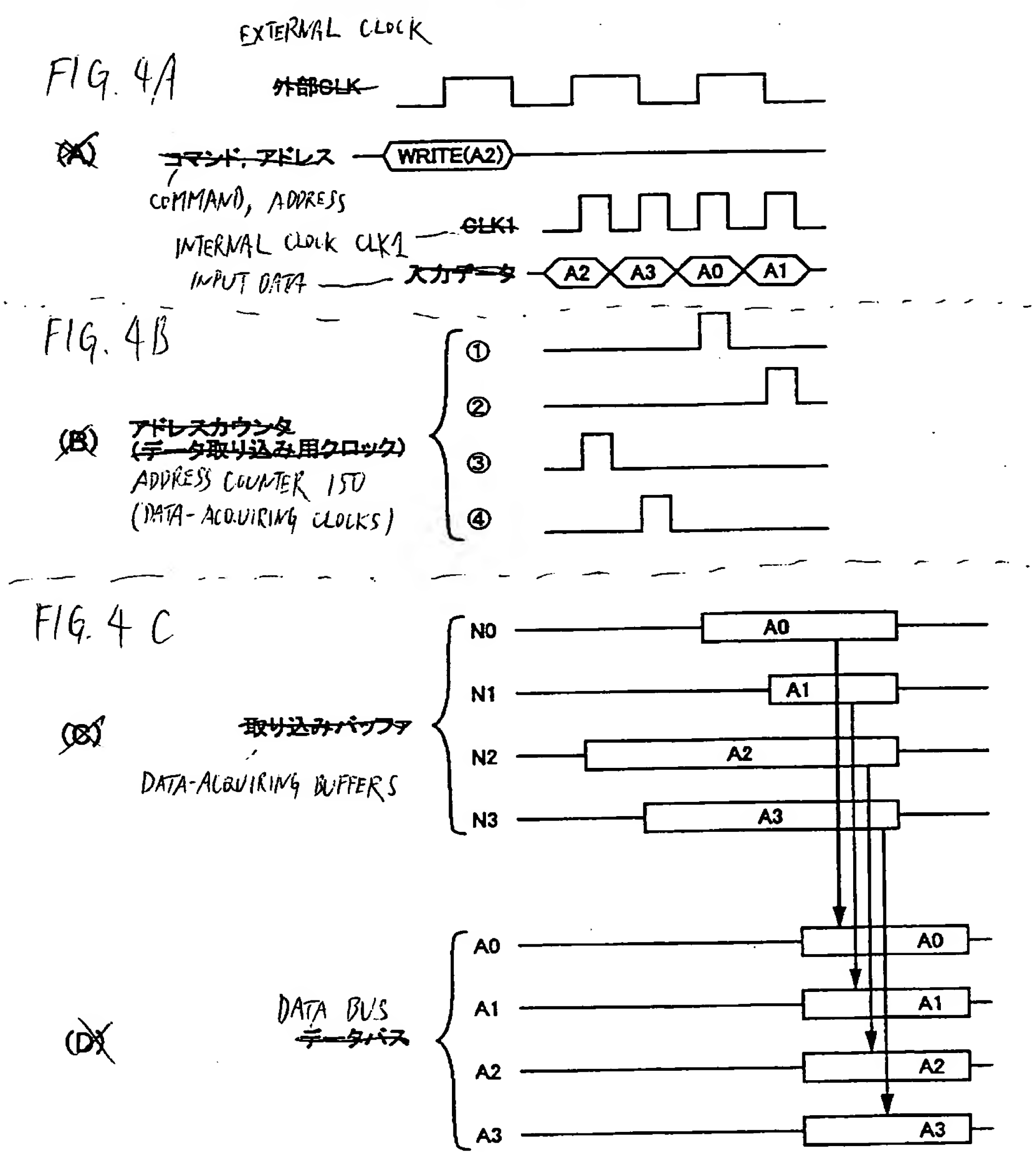
FIG. 3

~~入力回路の他の一例の構成図~~



【~~図4~~】

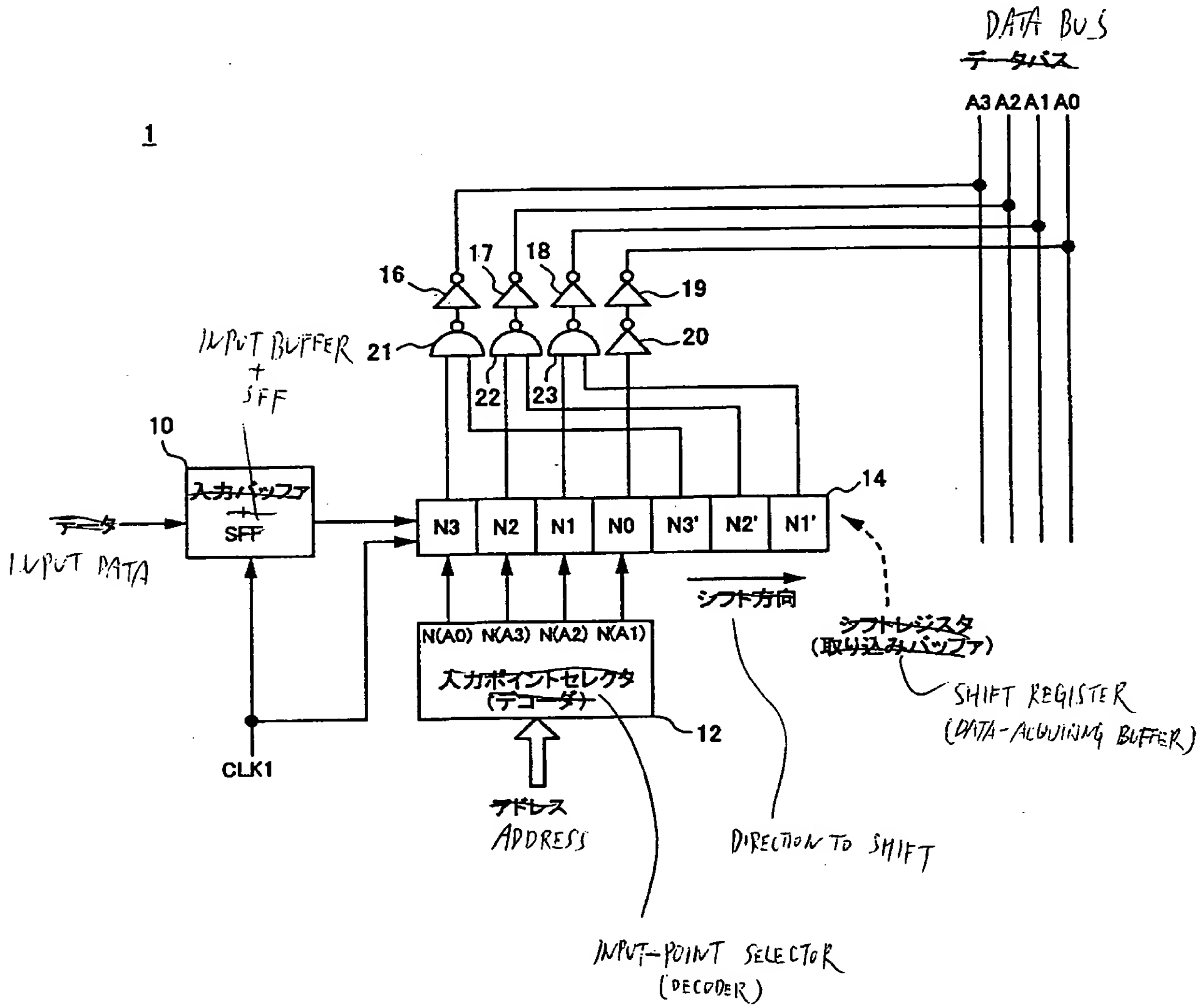
~~入力回路の動作を説明する図~~



~~【図５】~~

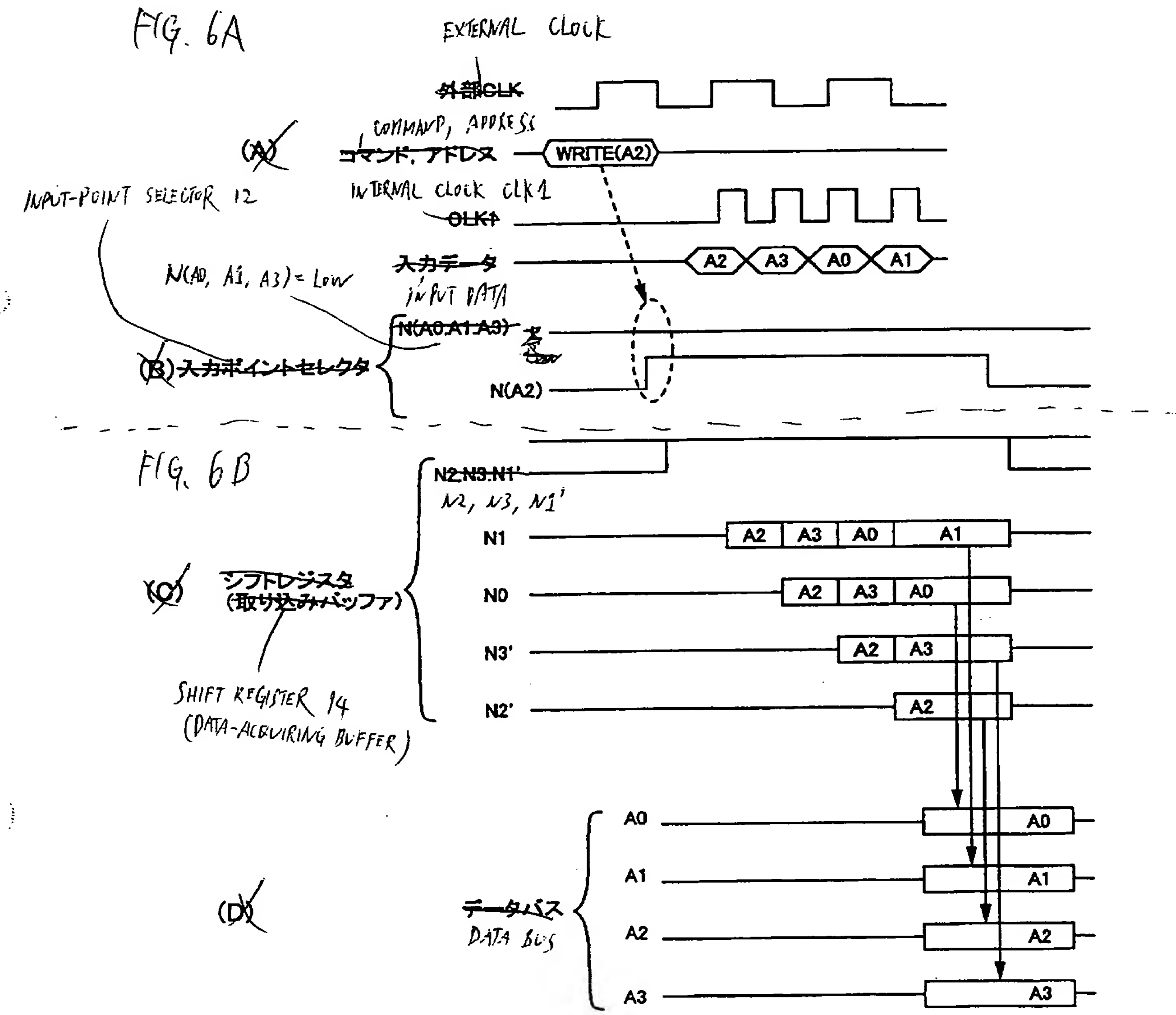
FIG. 5

~~本発明の入力回路の第1実施例の構成図~~



【~~図6~~】

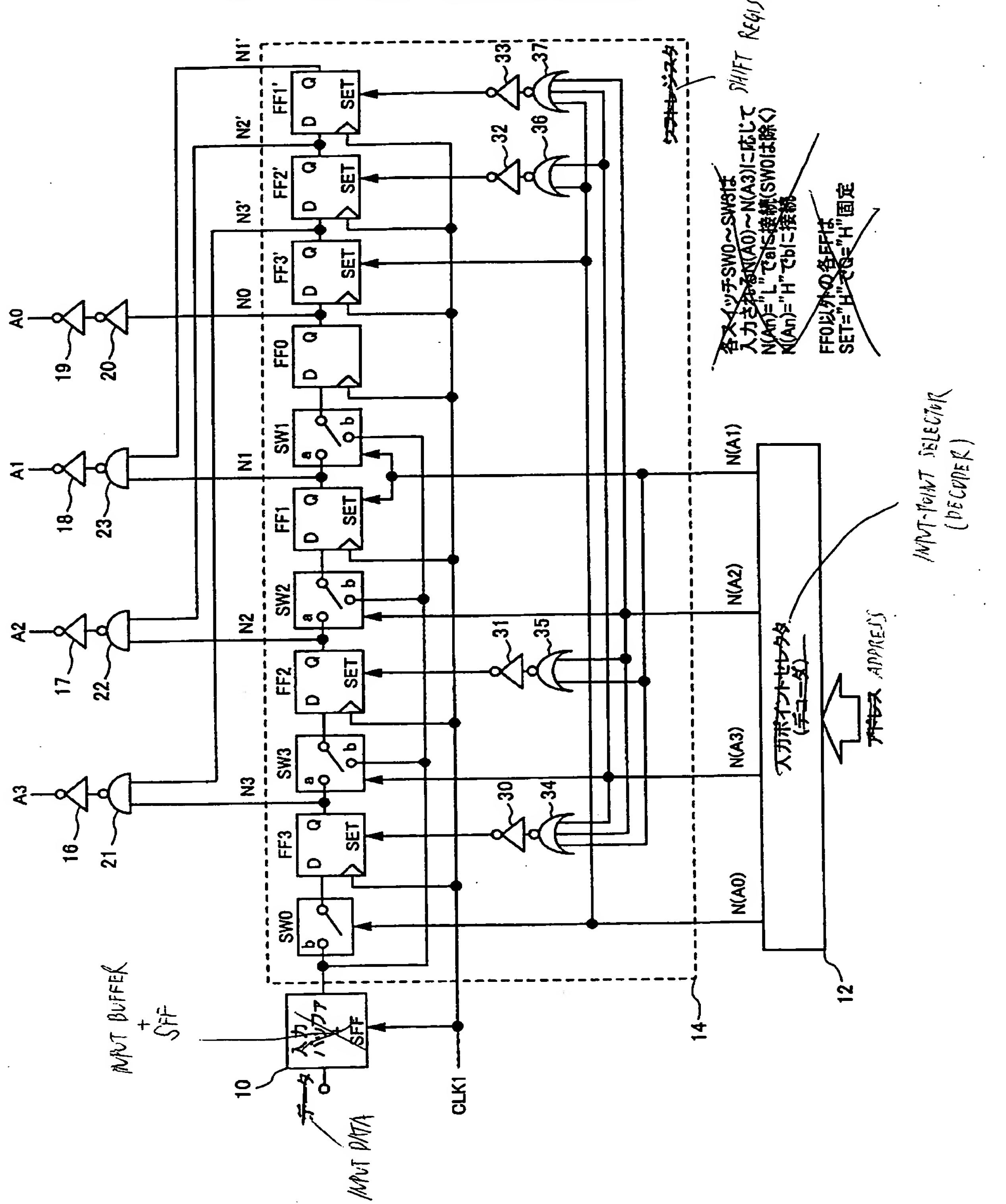
~~本発明の入力回路の動作を説明する一例の図~~



~~【図７】~~

~~シフトレジスタの一実施例の構成図~~

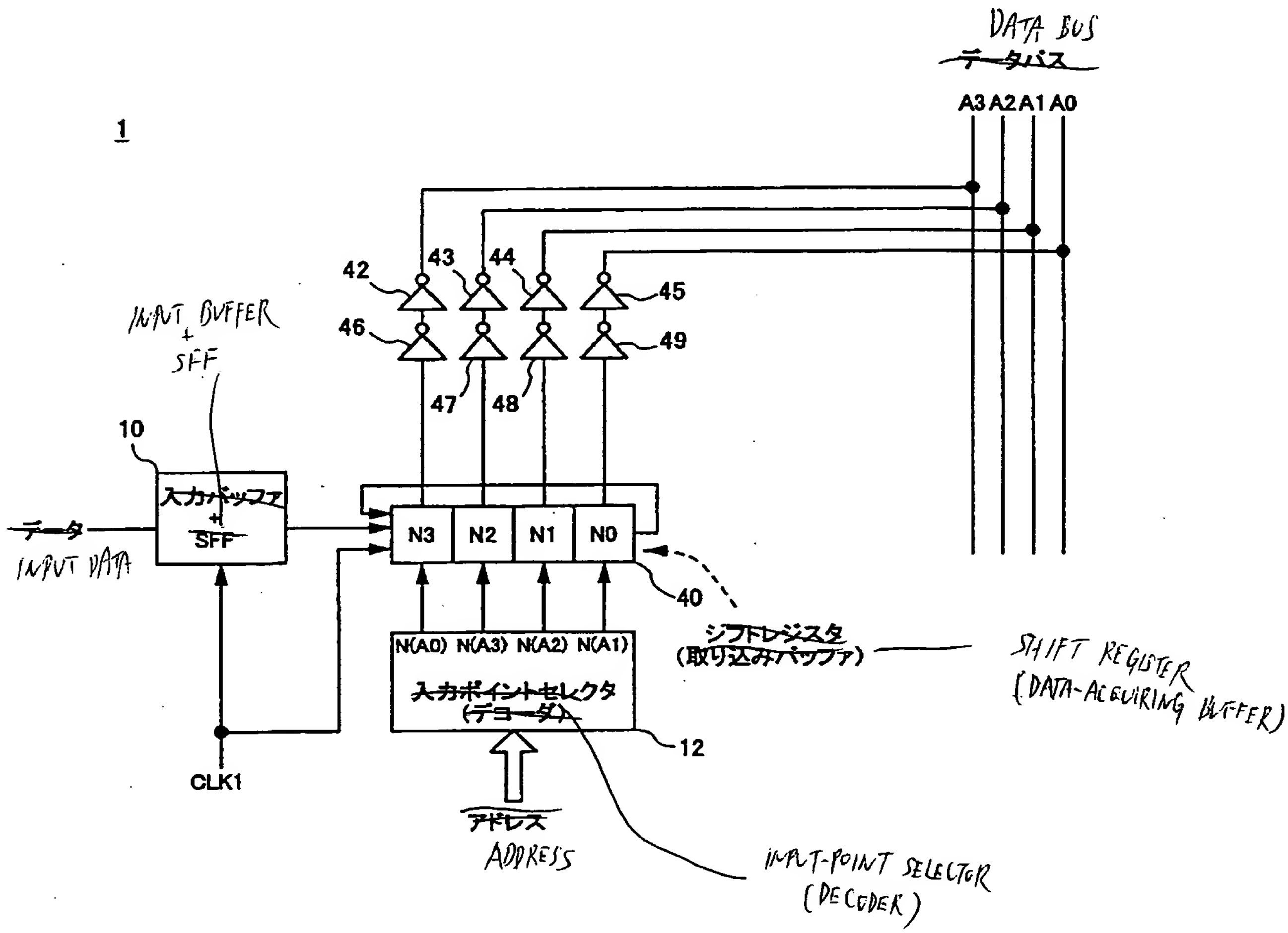
FIG. 7



~~【図８】~~

FIG. 8

~~本発明の入力回路の第2実施例の構成図~~



~~【図 9】~~

~~本発明の入力回路の動作を説明する一例の図~~

FIG. 9A

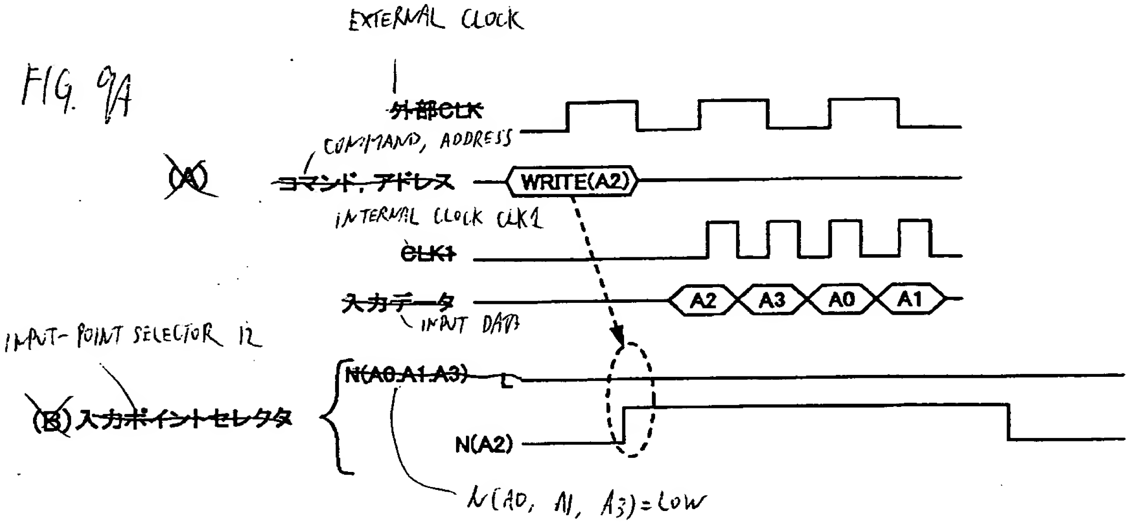
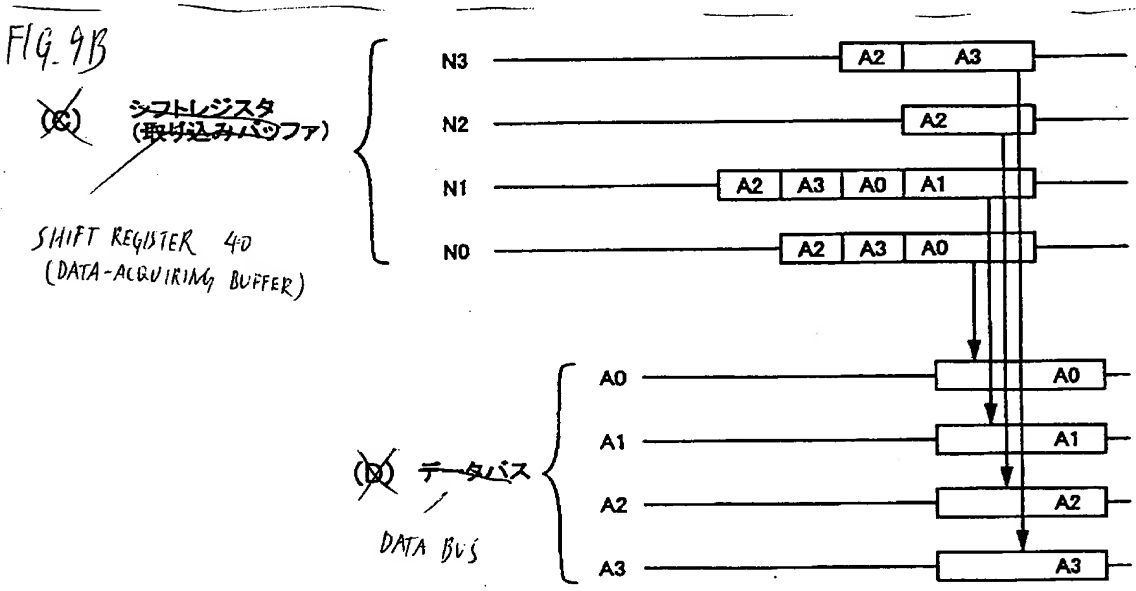


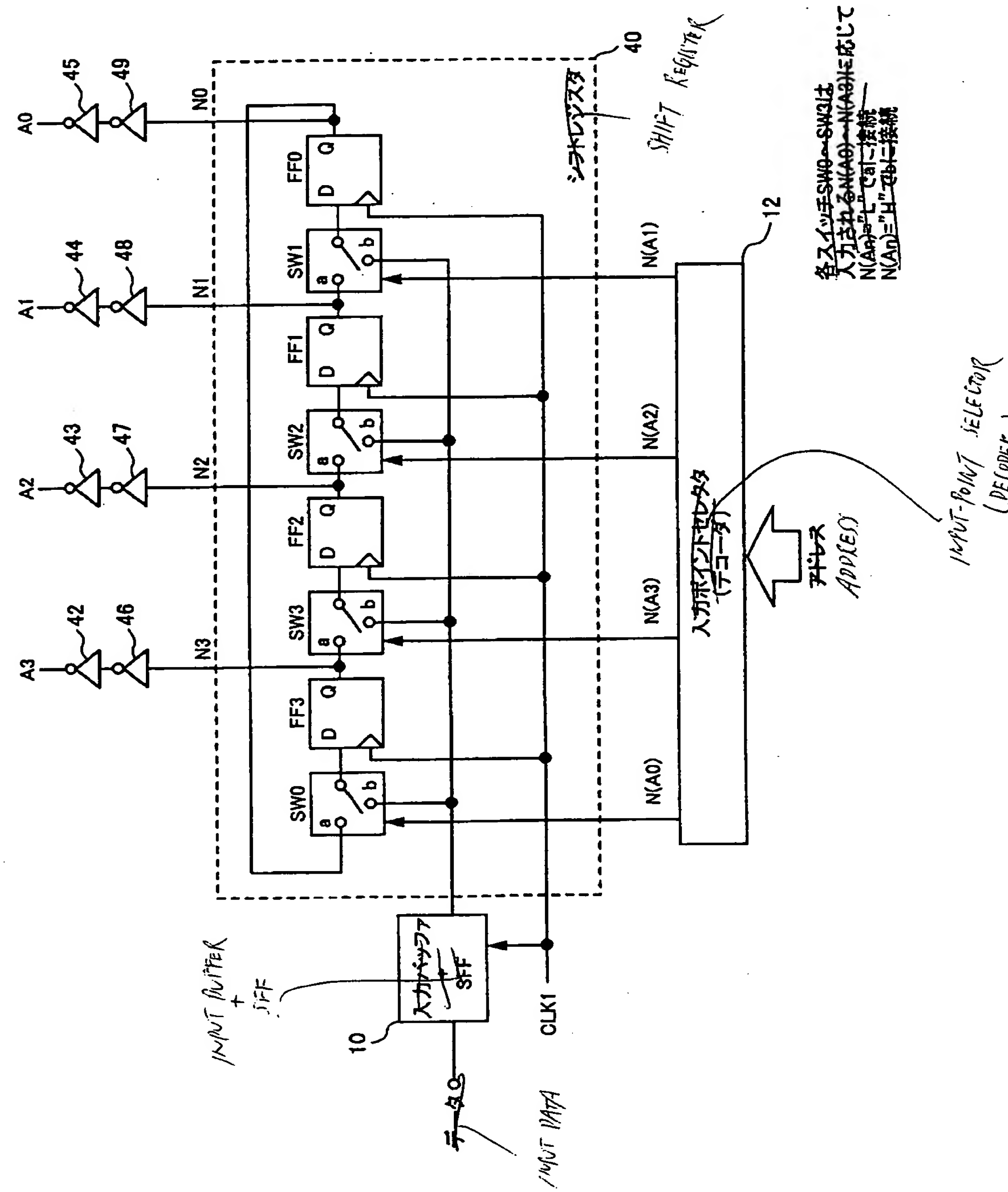
FIG. 9B



~~【図１０】~~

~~シフトレジスタの一実施例の構成図~~

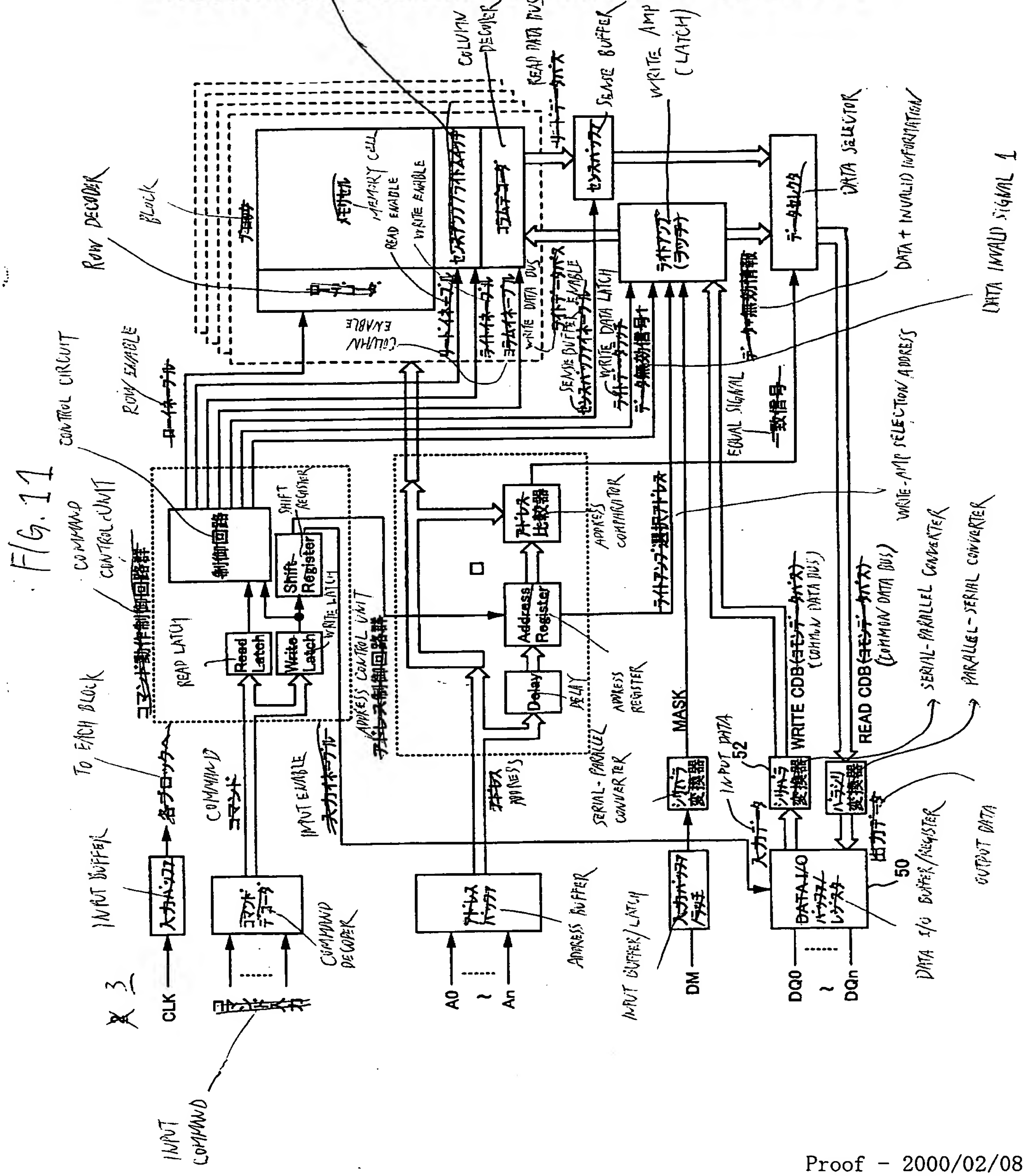
F/G. 10



~~【図１１】~~

~~本発明の入力回路を利用する半導体装置の一例の構成図~~

FIG. 11



[Name of Document] ABSTRACT

[Abstract]

[Problem to Be Solved] It is an object of the present invention to provide a data input circuit with a reduced size, a simplified configuration, and an increased operation speed, and a semiconductor device including such data input circuit.

[Solution Means] The above object is achieved by implementing data shifting means 14 that sequentially shifts an order of input serial data , and selection means 12 that selects a column of the data shifting means 14 that inputs the serial data according to an address signal.

[Selected Drawing] FIG. 5